Computer Architecture & Microprocessor

Subject Code: 28553

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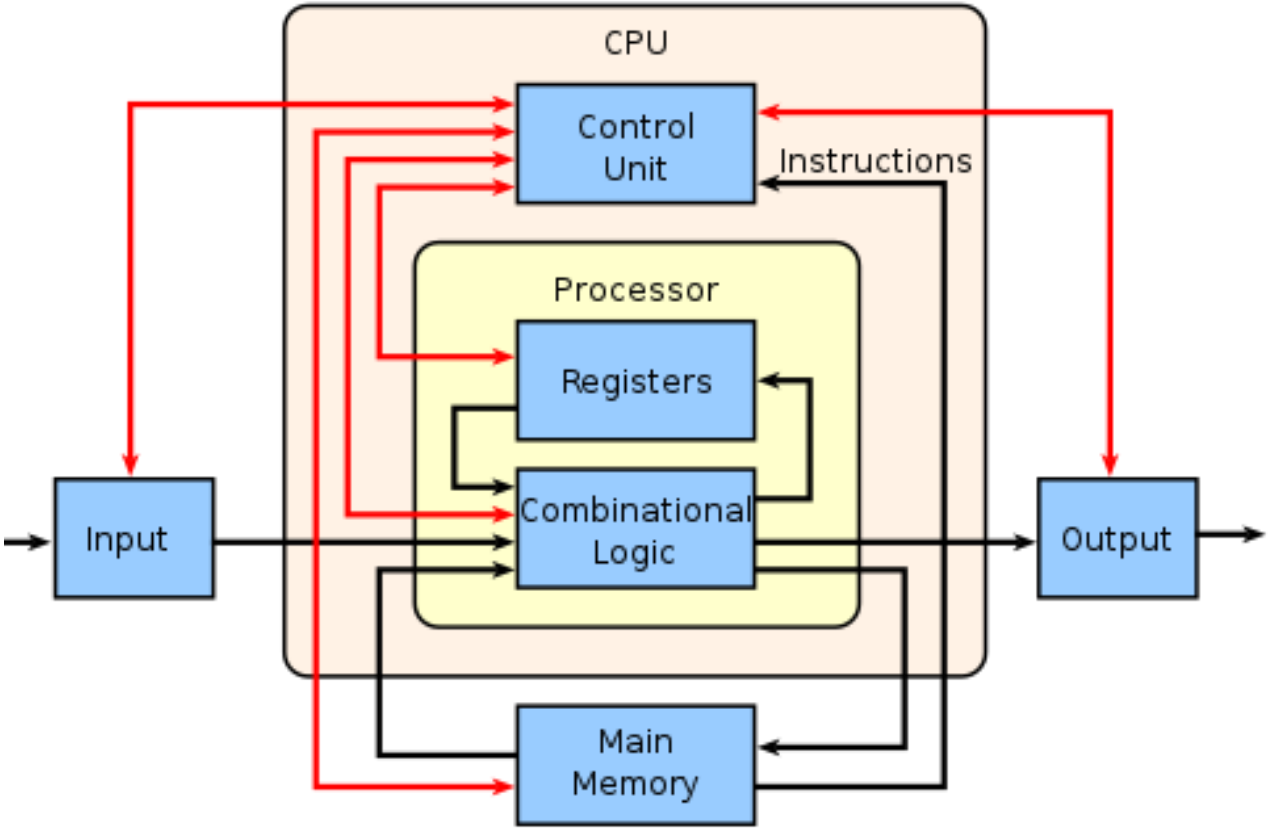
Chapter-1

Architecture of Simple As Possible Computer (SAP-1)



Simple As Possible Computer (SAP-1)

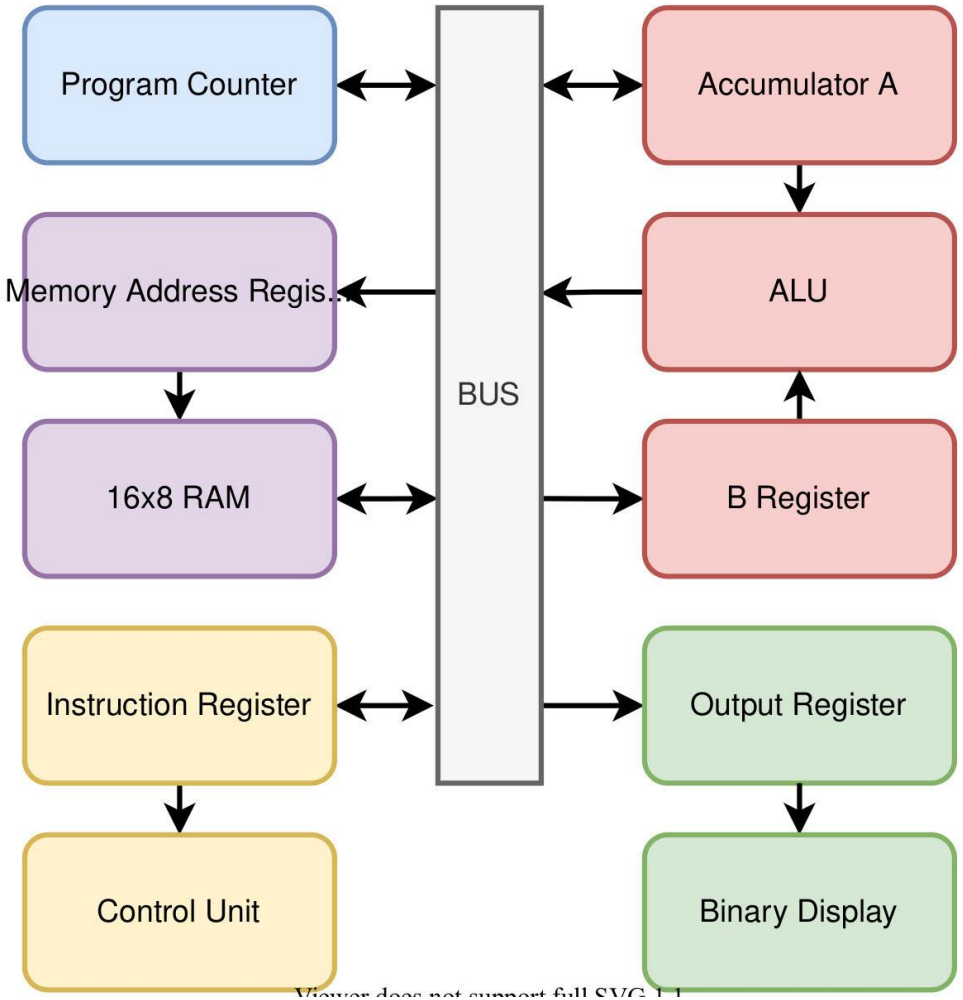


Figure of SAP-1

Description of SAP-1

- The **Simple-As-Possible** (SAP) computer is a simplified computer architecture designed for educational purposes and described in the book *Digital Computer Electronics* by Albert Paul Malvino and Jerald A. Brown.
- The SAP architecture serves as an example in *Digital Computer Electronics* for building and analyzing complex logical systems with digital electronics.

- *Digital Computer Electronics* successively develops three versions of this computer, designated as SAP-1, SAP-2, and SAP-3. Each of the last two build upon the immediate previous version by adding additional computational, flow of control, and input/output capabilities. SAP-2 and SAP-3 are fully Turing-complete.
- The instruction set architecture (ISA) that the computer final version (SAP-3) is designed to implement is patterned after and upward compatible with the ISA of the Intel 8080/8085 microprocessor family.

Chapter-2
Basics of Computer Architecture

- A stored-program computer is a computer that stores program instructions in electronically or optically accessible memory. This contrasts with systems that stored the program instructions with plugboards or similar mechanisms.
- The concept of the stored-program computer can be traced back to the 1936 theoretical concept of a universal Turing machine. Von Neumann was aware of this paper, and he impressed it on his collaborators.

RISC VS CISC

	RISC	CISC
Instruction Set Complexity	Supports a smaller number of instructions that perform simpler operations.	Supports a wide variety of instructions for complex operations.
Instruction Format	Uses a fixed-length instruction format.	Can have variable-length instruction formats.
Pipeline Design	Has a simpler pipeline design.	Can have longer pipelines with more complex stages.
Memory Access	Relies on load/store architecture; memory access through load and store instructions.	Supports instructions that can directly operate on memory.
Performance and Optimization	Designed for executing instructions in a small number of clock cycles.	May require more clock cycles to execute instructions
Code Density	May require more instructions to perform a task, resulting in larger program sizes.	Can often perform more operations in a single instruction, leading to smaller program sizes.

ALU Unit

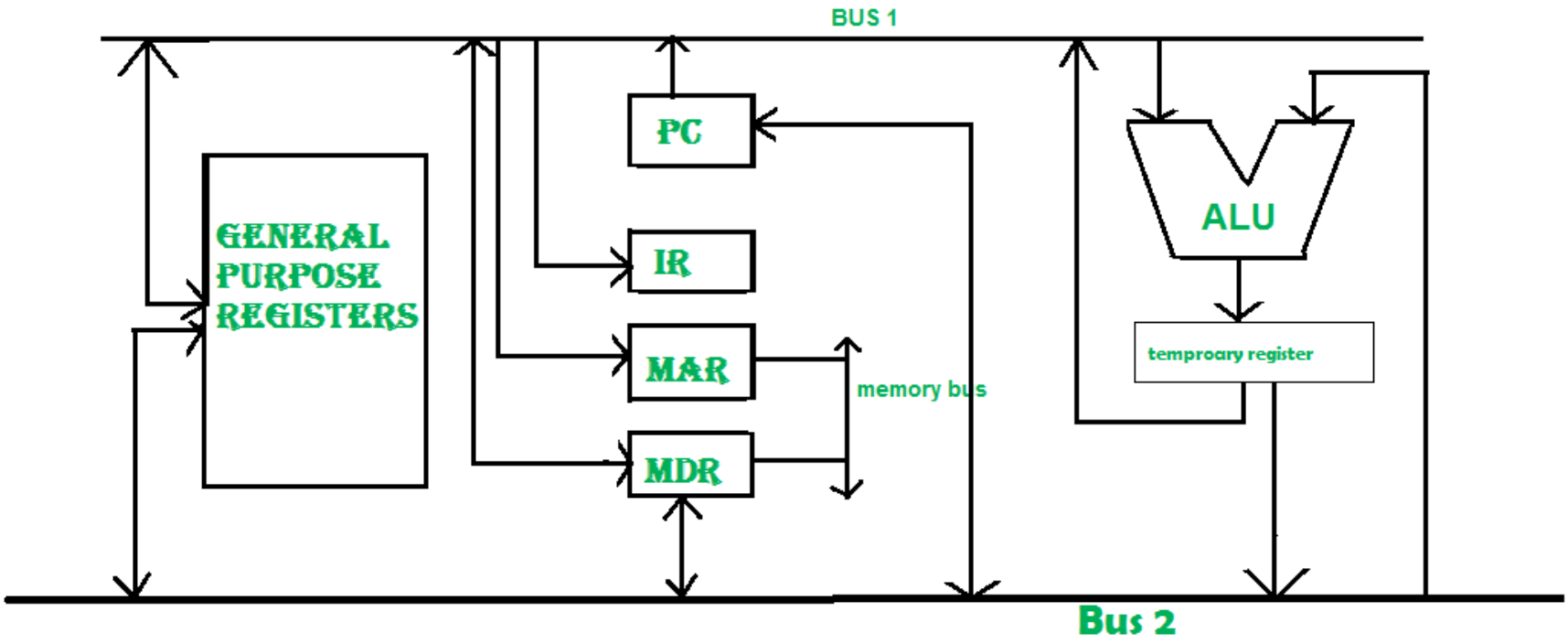
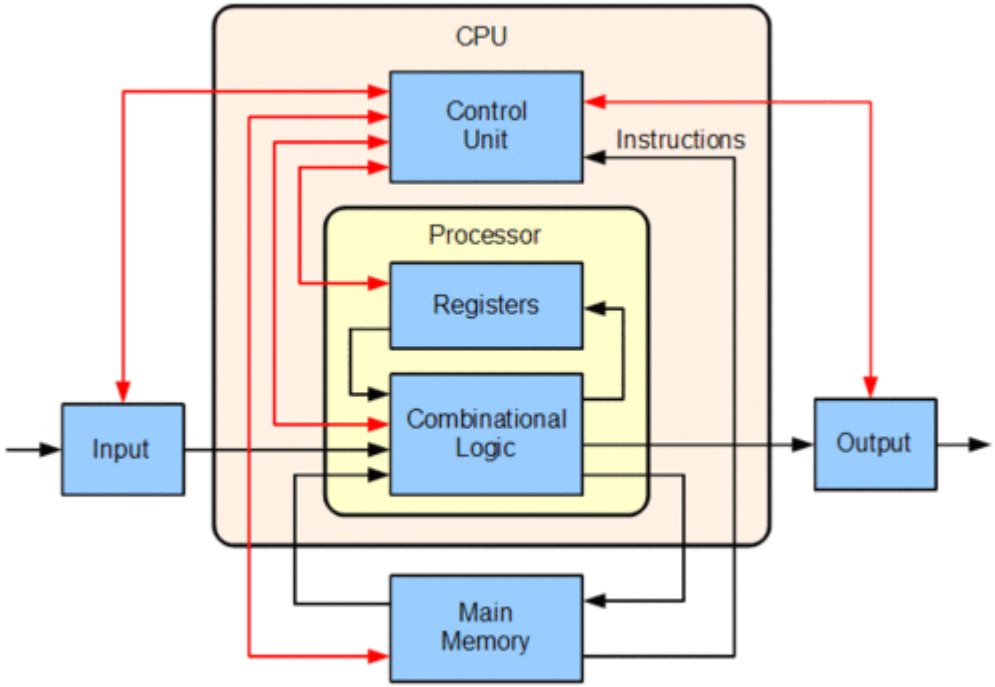


fig.TWO BUS ORGANISATION

- General purpose registers are extra registers that are present in the CPU and are utilized anytime data or a memory location is required.
- These registers are used for storing operands and pointers. These are mainly used for holding the following: Operands for logical and arithmetic operations
- In computing, an arithmetic logic unit (ALU) is a combinational digital circuit that performs arithmetic and bitwise operations on integer binary numbers.

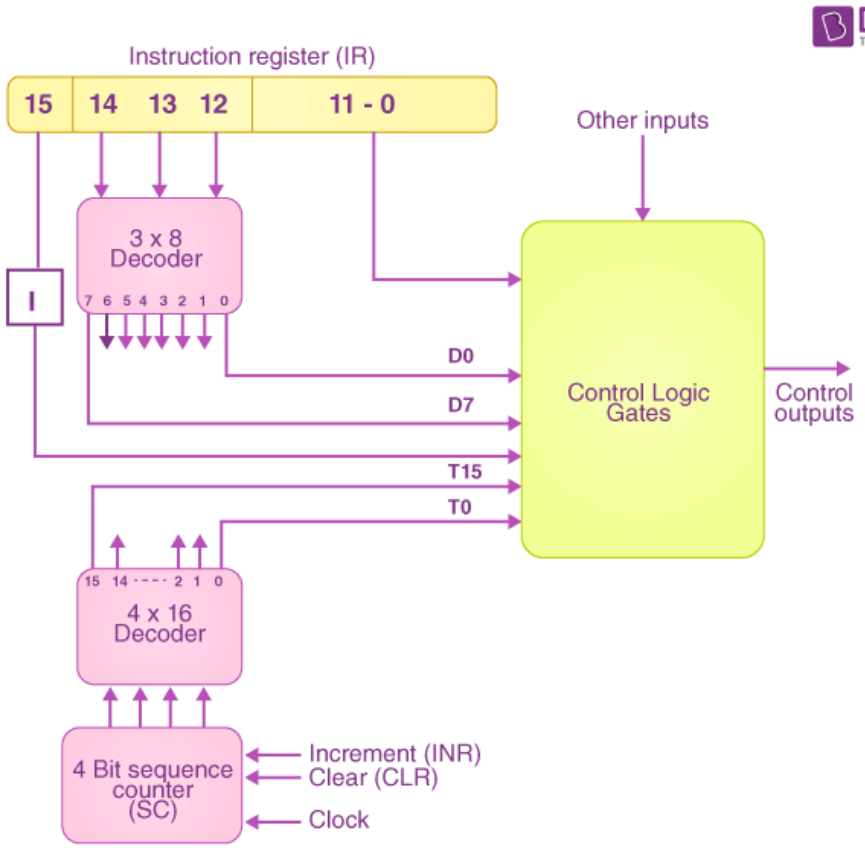
Chapter-3:
Basic of CPU Design



A CPU consists of all these parts

- General purpose Register
- Dedicated Register
- Arithmetic logic unit (Alu)
- Dedicated Hardware & firmware
- Control Unit

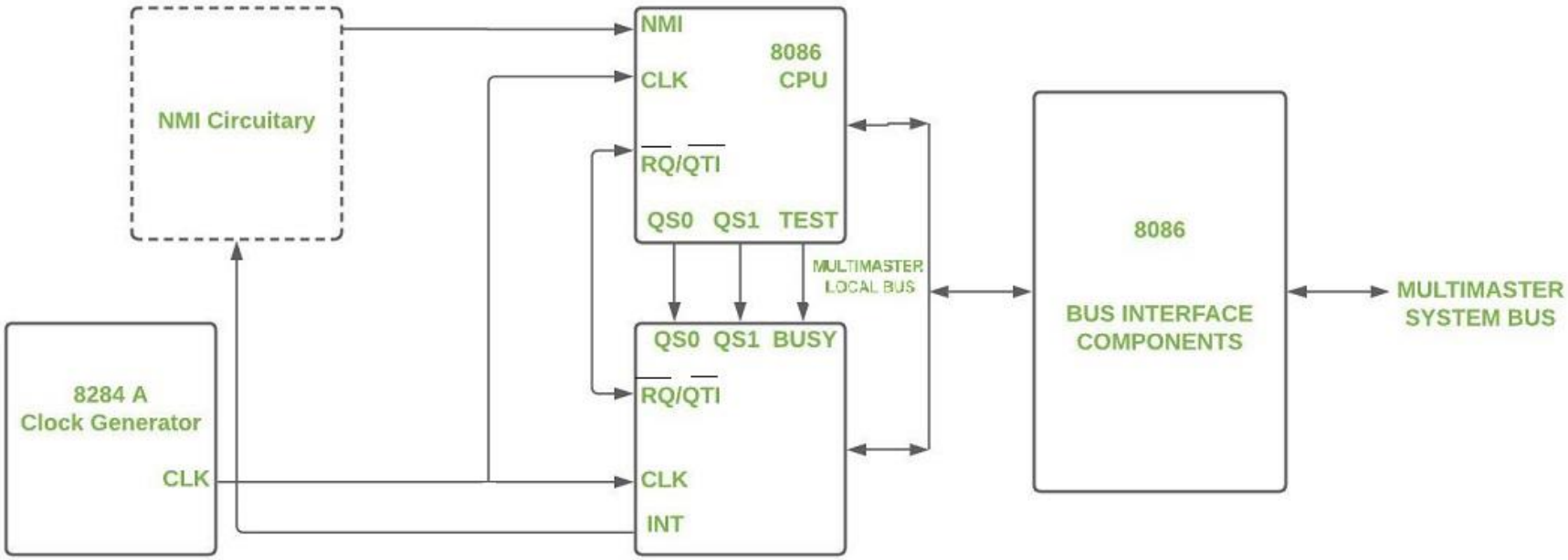
Illustrate Hardwired and Microprogramming Approach for Control Unit Design



Control Unit of a Basic Computer

- In computer architecture, the control unit is responsible for directing the flow of data and instructions within the CPU. There are two main approaches to implementing a control unit: hardwired and micro-programmed.
- A hardwired control unit is a control unit that uses a fixed set of logic gates and circuits to execute instructions. The control signals for each instruction are hardwired into the control unit, so the control unit has a dedicated circuit for each possible instruction.

Co-Processor Interfacing



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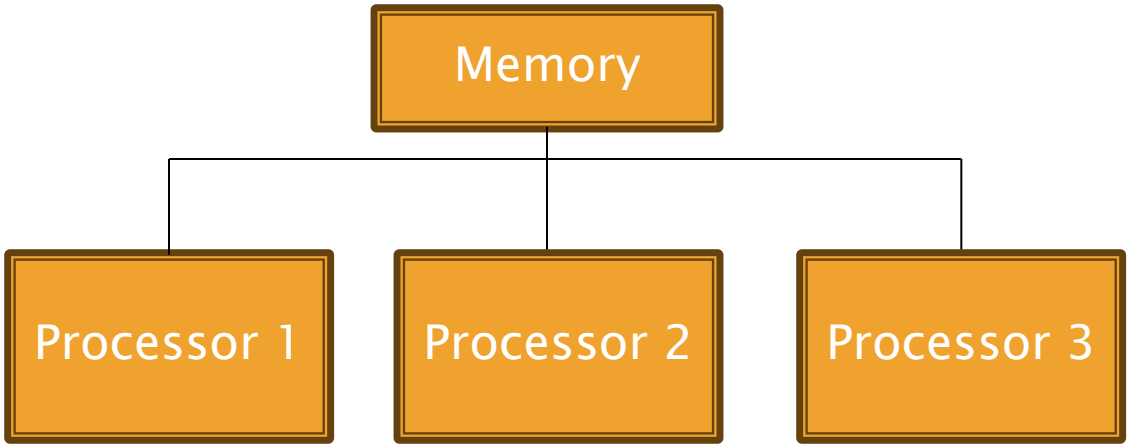
Chapter-4
Memory Organization & I/O sys.

- Topics:-

- Centralized memory organization.
- Distributed memory organization.
- Design 4k * 4Programmed I/O, Interrupt I/O and DMA.
- RAM using four 1k*4RAM chips

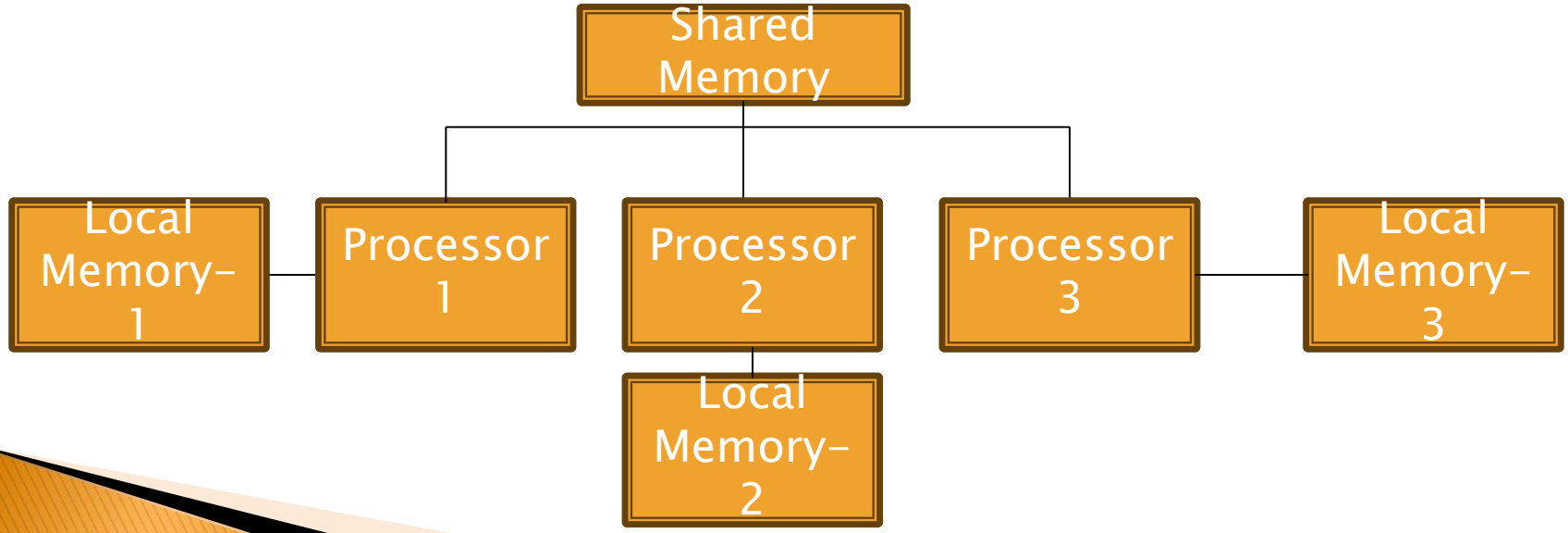
Centralized memory organization

- Centralized memory organization refers to a system architecture where there is a single, central memory unit shared by all components, such as the CPU and peripheral devices

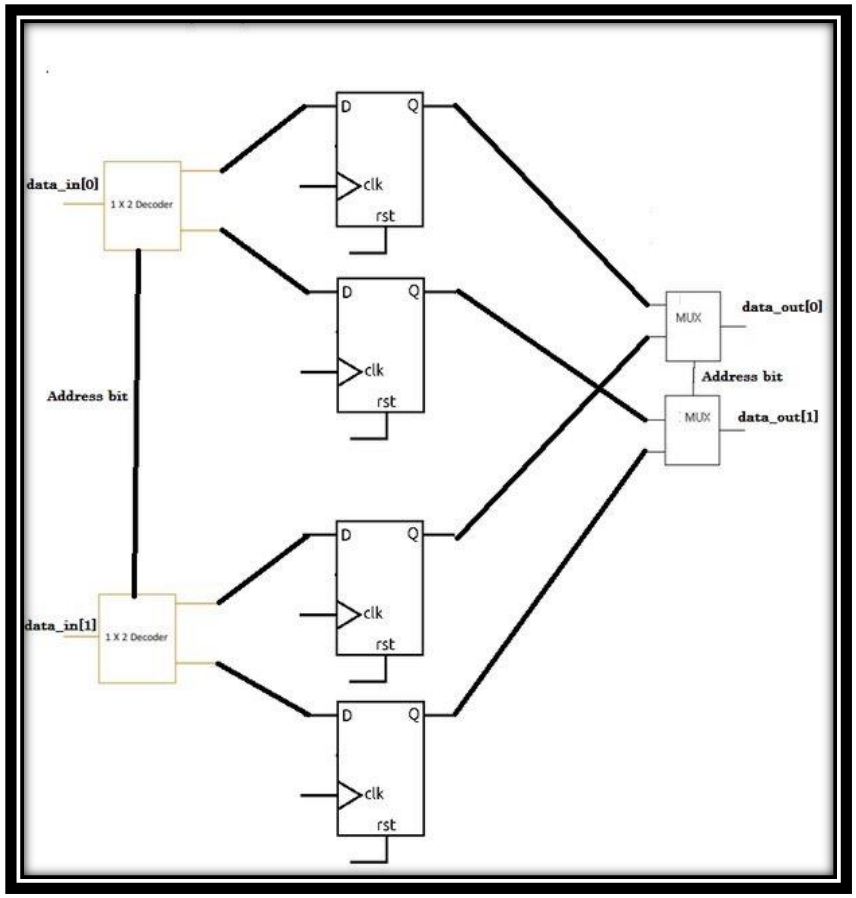


Distributed memory organization :

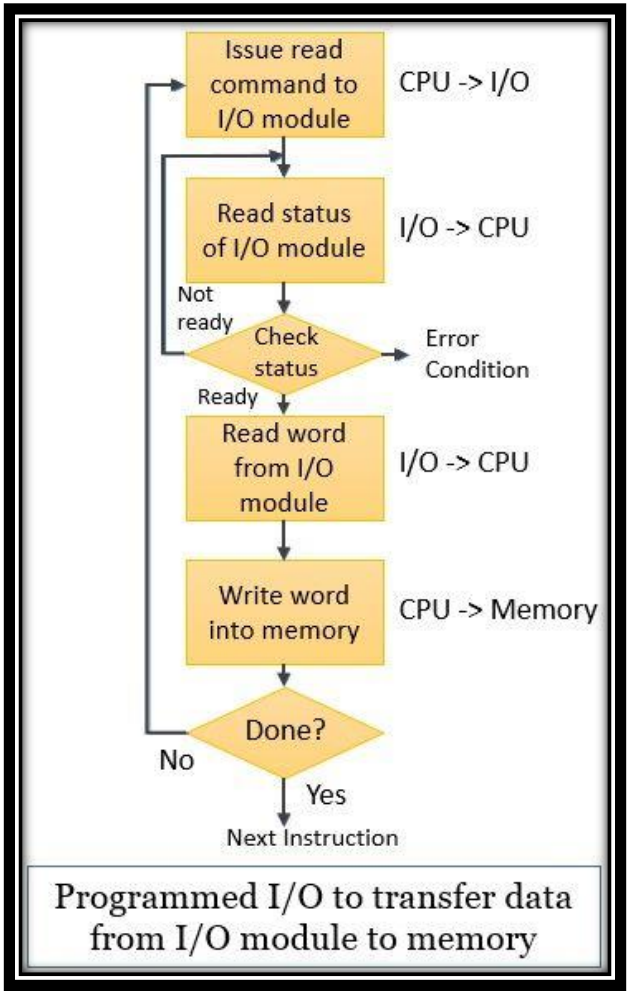
- Distributed memory organization refers to a system architecture where different components have their own independent memory units, rather than relying on a single, central memory.



Design 4k * 4 RAM using four chips :

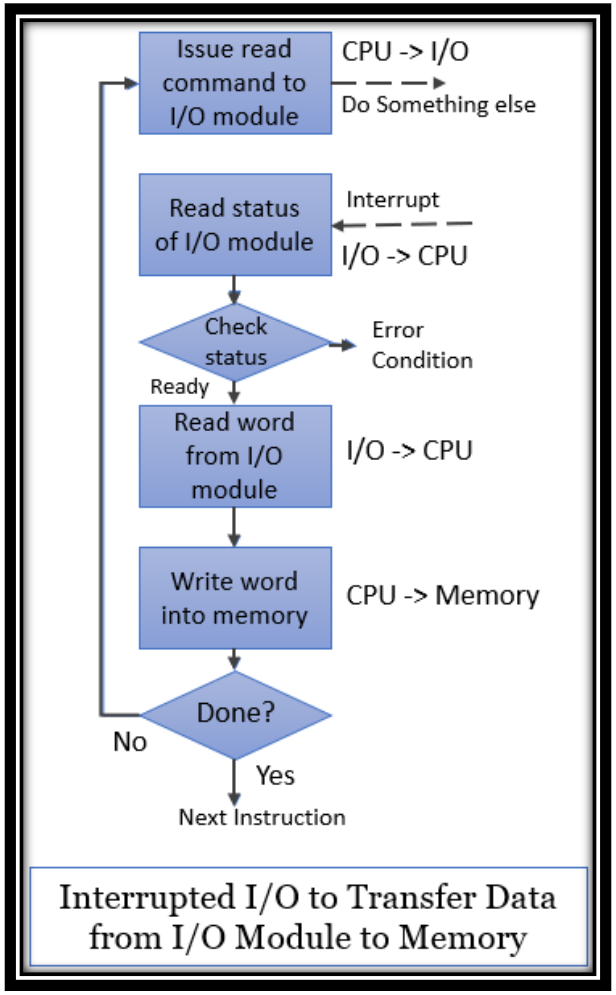


Programmed I/O:

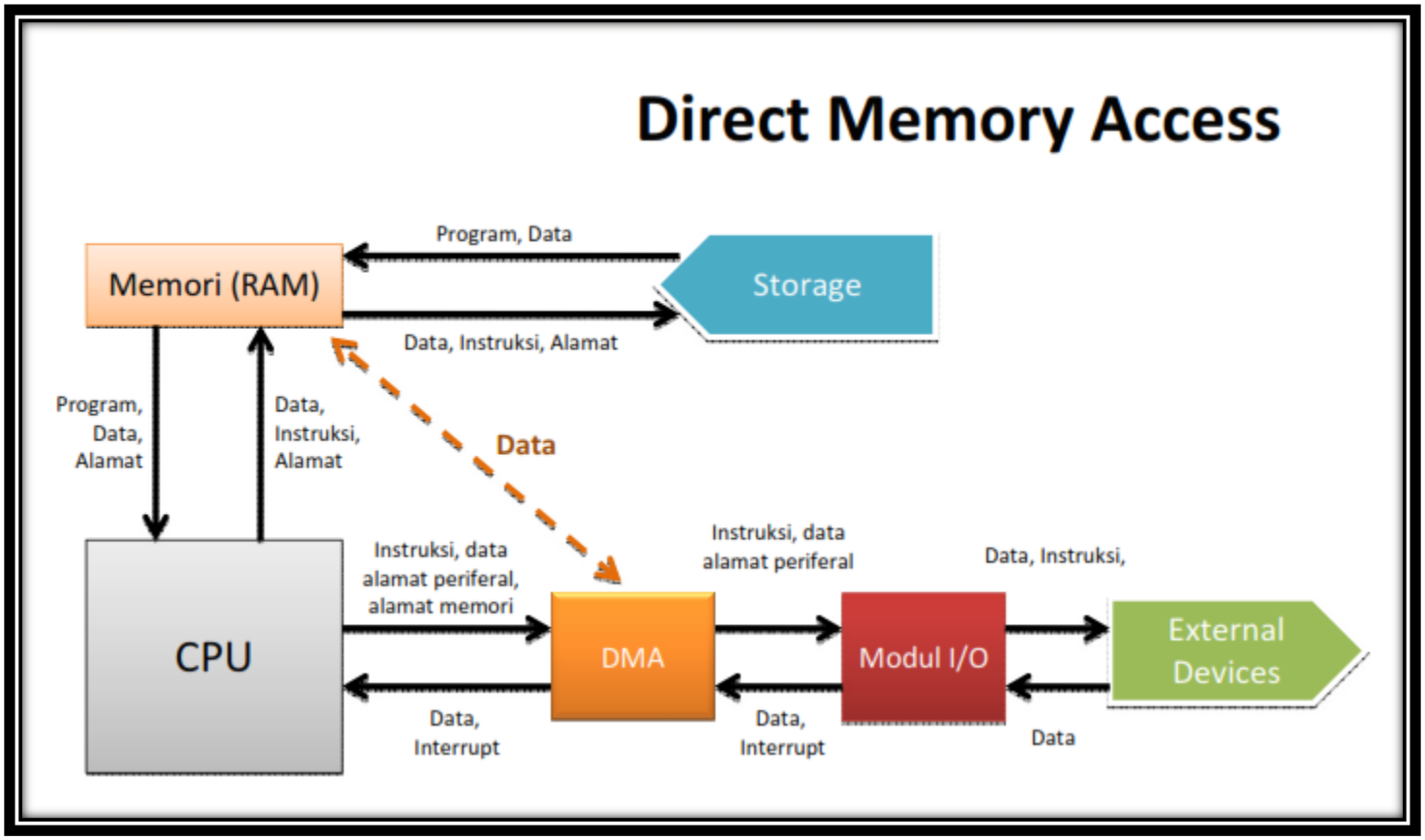


Programmed I/O to transfer data from I/O module to memory

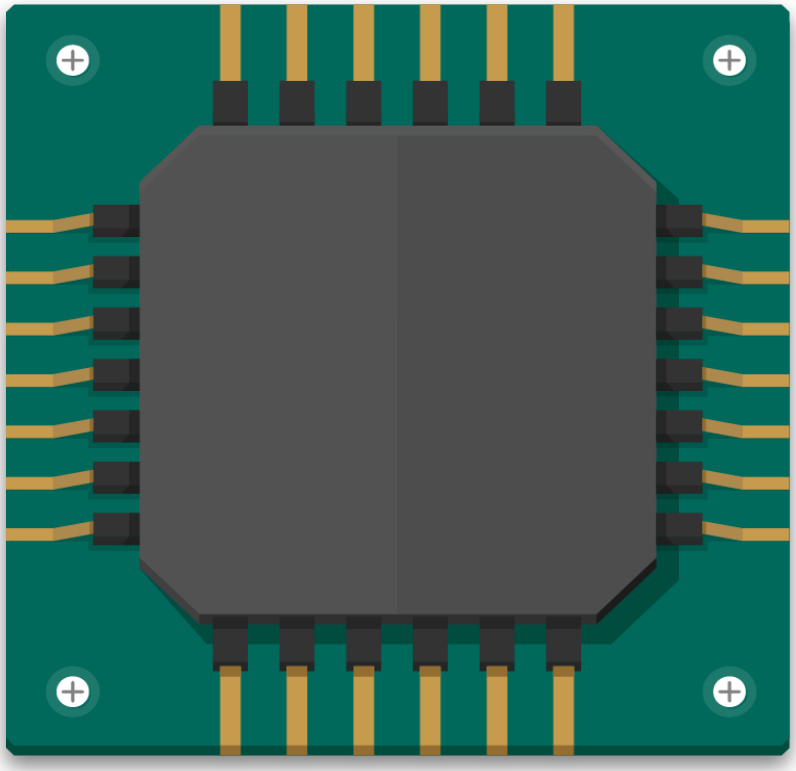
Interrupt I/O:



Direct Memory Access (DMA):



Chapter-5:
Architechture of 8085 Microprocessor



The architecture of the Intel-8086 microprocessor :

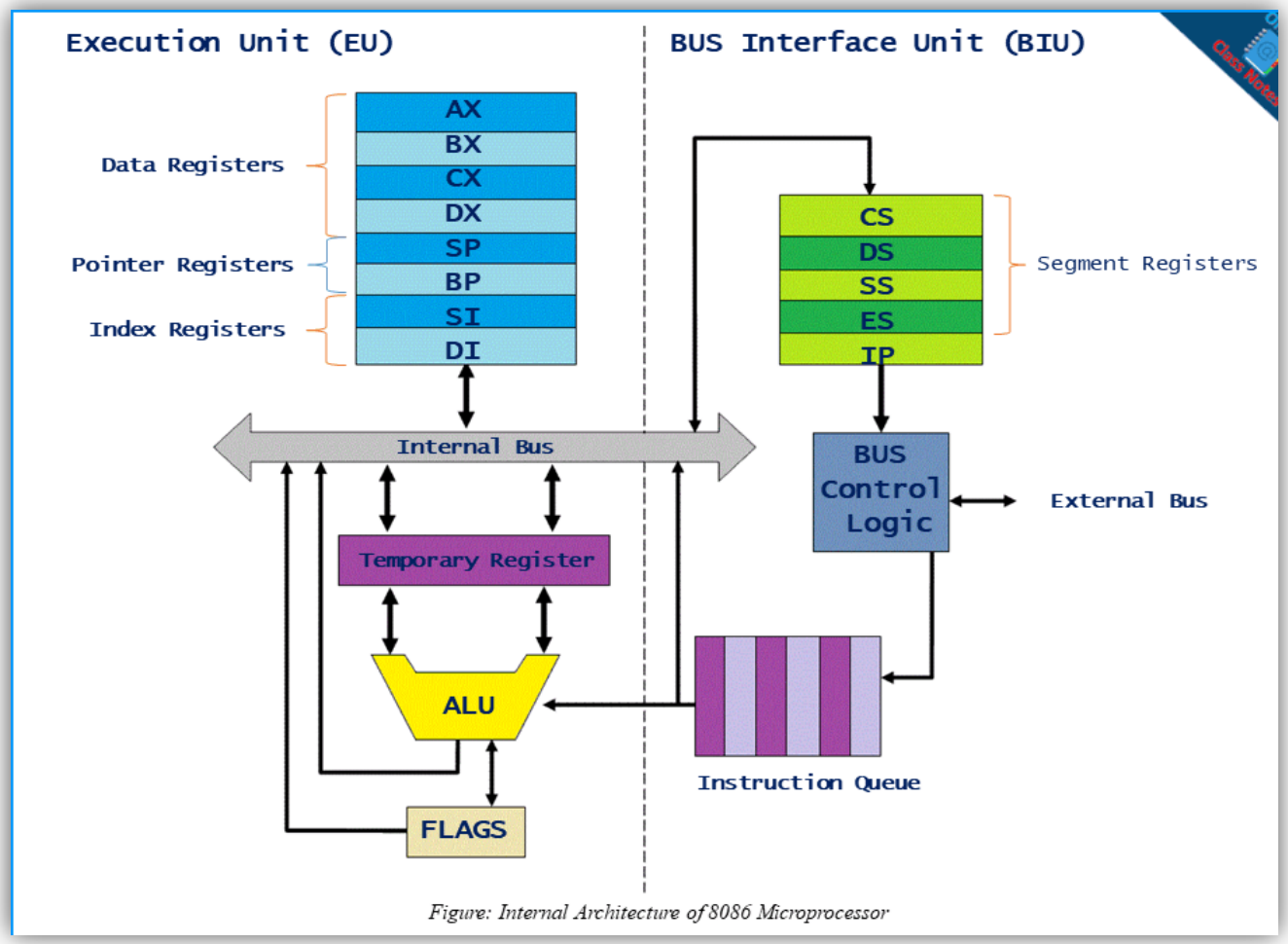


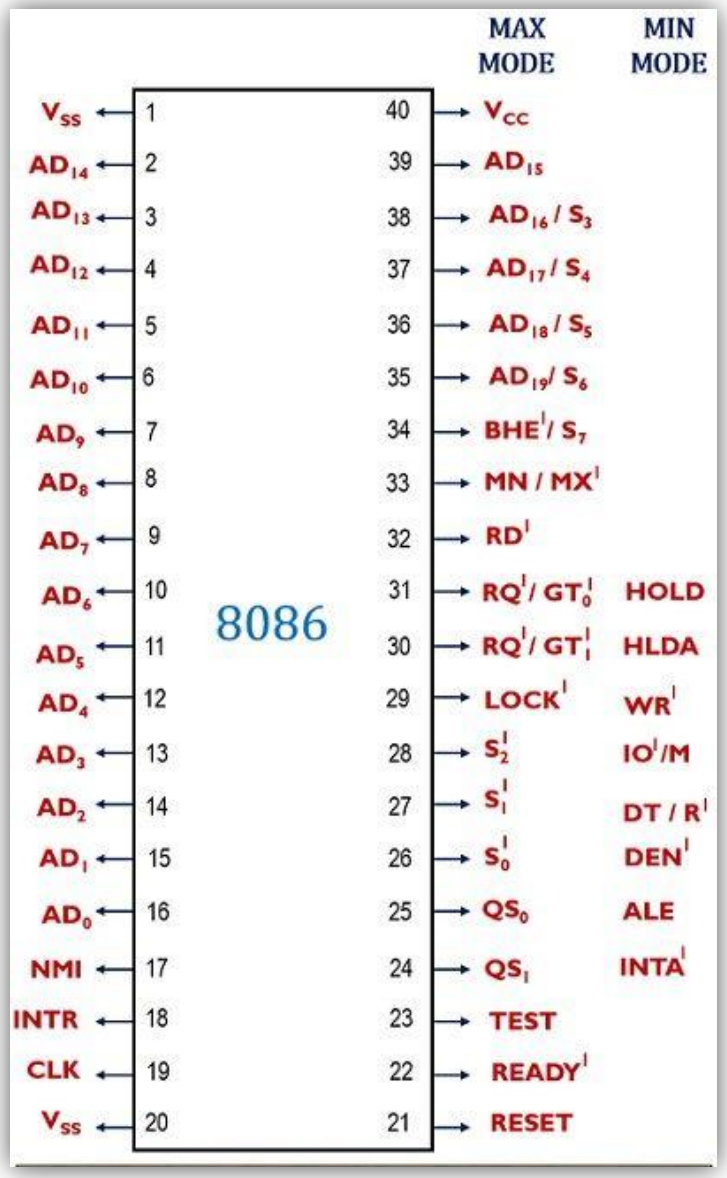
Figure: Internal Architecture of 8086 Microprocessor

- The 8086 microprocessor has a segmented memory architecture, which means that memory is divided into segments that are addressed using both a segment register and an offset.
- The segment register points to the start of a segment, while the offset specifies the location of a specific byte within the segment.

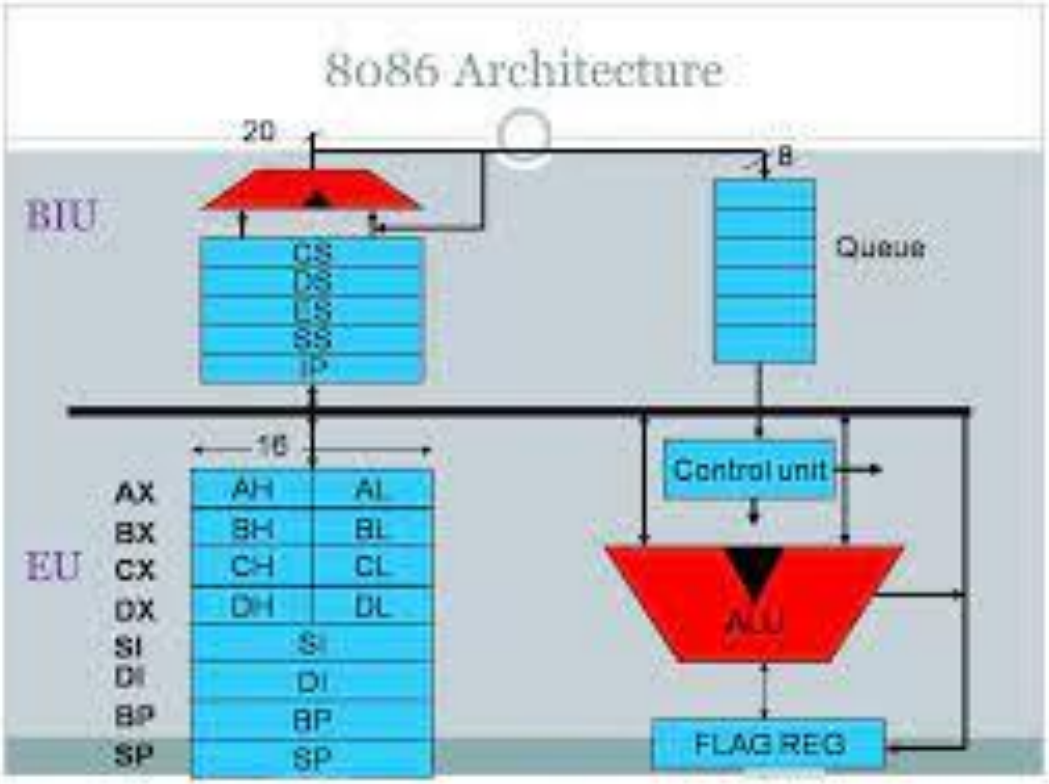
Pin diagram with function of each pin of 8086 microprocessor:

Pin functions:

- CLK: Clock Input.
- MN/MX: Minimum/Maximum Mode Control. MN=0 for minimum mode, MN=1 for maximum mode.
- BHE: Bus High Enable. When BHE is active, the upper byte of the data bus (D8-D15) is enabled during read/write operations. 4-19. A19-A4: Address Lines. 20-27. A3-A10: Additional Address Lines. 28-35. AD0-AD7: Data Bus (8-bit bidirectional data lines). 36-39. AD8-AD15/S0-S3: Additional Data Bus and Status Lines.
- VCC: Power supply voltage.



8086icroprocessor archtecher



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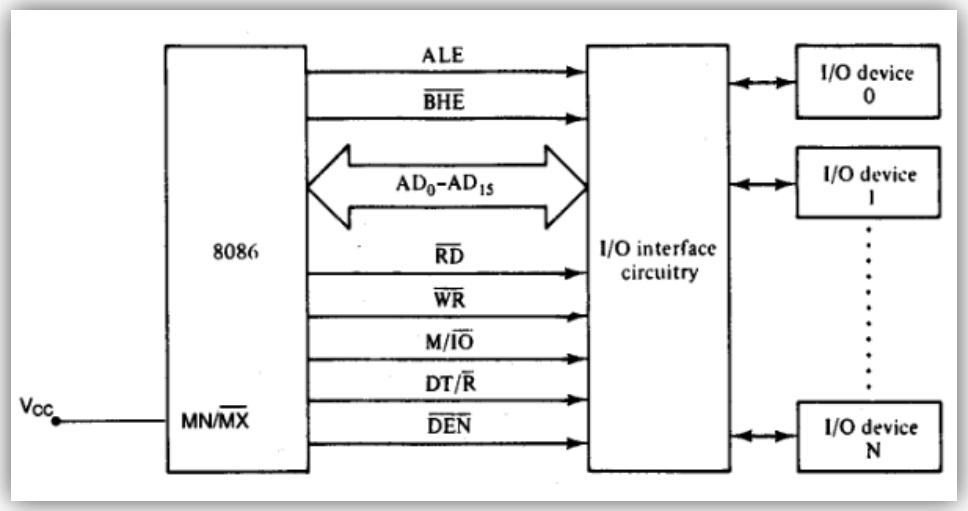
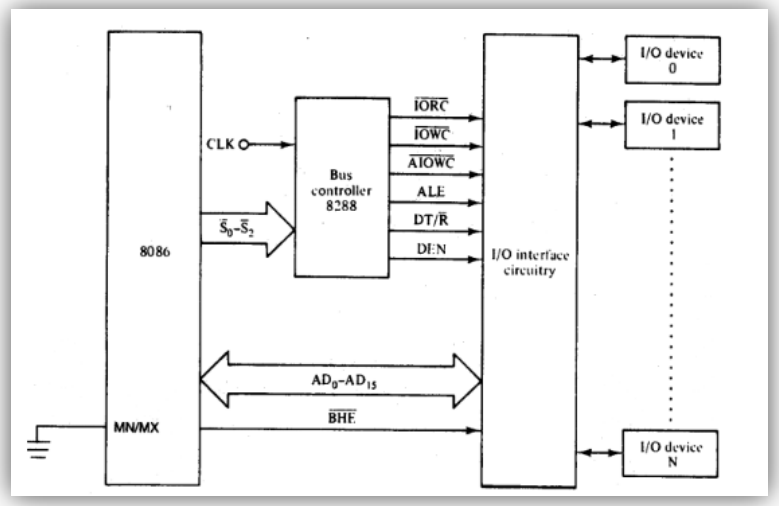
Minimum & Maximum mode of the 8086 microprocessor:

Minimum



Maximum



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